2024

COMPUTER SCIENCE — HONOURS

Paper : DSCC-1

(Computer Fundamentals and Digital Logic)

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer ***any five*** questions : 2×5

(a) Draw the Karnaugh map for the following Boolean expression :

$$x = \overline{A} \cdot B + \left(B + \overline{C}\right) \cdot A$$

(b) What is the principle of duality?

(c) Define Fan-Out with respect to TTL circuits.

(d) What is the difference between system software and application software?

(e) How can you implement an XOR logic function using just four two-input NAND gates? Illustrate with the necessary circuit diagram.

(f) Highlight four main differences between combinational and sequential circuit.

(g) What is weighted code? Differentiate between weighted and non-weighted code.

(h) What role does a de-bouncer circuit play in a digital circuit system?

Answer ***any three*** questions.

2. (a) State De-Morgan's theorem.

(b) Realize OR logic function using NAND logic gates only. 2+3

3. Simplify the Logic expression $y = \Sigma_m (0, 2, 4, 6, 8) + \Sigma_d (1, 7, 9, 15)$ using a Karnaugh map (K-map). Draw the truth table and design the circuit using the simplified expression. 2+3

4. Draw the circuit diagram of a TTL NAND gate and provide a brief explanation of how it operates. Define floating input with respect to TTL Logic gates. 4+1

5. Design a 3-bit full adder with logic gates. Draw the truth table. 3+2

6. Compose a brief note on any topic of your choice : 5

   (a) Race around condition

   (b) Clocked D-flip-flop

   (c) Secondary memory devices.

Answer ***any five*** questions.

7. Implement the function F (A, B, C, D) = Σ_m (1, 2, 6, 8, 9, 12) using a 8 to 1 multiplexer along with other required logic gates. Explain the design process, create the truth table, derive the simplified expression and provide the logical circuit diagram. 3+2+3+2

8. What is a 3-bit full subtractor? Illustrate its truth table, derive simplified logical expressions for the Difference and Borrow outputs, and design the logical circuit using only NAND gates. 2+2+3+3

9. Design an asynchronous BCD counter using JK flip-flop, and provide the corresponding truth table along with logical circuit diagram. 4+3+3

10. (a) Design a parity cheeker and generator logic circuit for 3-bit data.

    (b) Why is a multiplexer considered a functionally complete circuit? Explain with appropriate illustrations. 4+6

11. (a) Realize the function $Y = \Sigma_m$ (1, 2, 5, 6) using a 3 to 8 decoder along with necessary logic gates. Draw the appropriate logic circuit diagram.

    (b) Design a circuit that can multiply a 2-bit number by another 2-bit number using only basic logic gates. Draw the logical circuit diagram. (3+2)+(3+2)

12. Design a 4-input, 3-output priority encoder where one of the outputs serves as a valid input indicator that remains high whenever any of the inputs are active. Explain the design procedure, draw the truth table, derive the simplified expression using Karnaugh map, and draw the appropriate logical circuit diagram. (3+2+3+2)

13. Design a BCD adder using a parallel adder and additional necessary logic gates. Discuss the need for a correction circuit, explain the design process, provide the truth table, and derive the logic circuit diagram. 2+3+2+3

14. (a) Design a 4-bit serial in serial out (SISO) register using negative edge triggered D-filp-flops, write the functional table and draw the appropriate logic circuit diagram.

    (b) Design a clocked/gated J-K flip flop using NAND logic gates only. Explain its operation, draw the truth table and appropriate logic circuit diagram. (2+2)+(2+2+2)
